Product Overview

The CX500 is a fully integrated single chip impulse radio Ultra Wide Band (UWB) SoC chip with features of low-power consumption, high integration, high performance, high security, and is compliant to IEEE802.15.4a HRP, IEEE802.15.4z HRP, FiRa, CCC and ICCE protocols. CX500 supports ranging, AoA (Angle of Arrival), radar and data transmitting. With small package of QFN40 (5mm*5mm), CX500 is especially suitable for automotive applications.

Key Feature

- IEEE802.15.4a HRP/IEEE802.15.4z HRP/FiRa/CCC/ICCE compliant
- Supports 500M channel bandwidth from 6 GHz to 9 GHz (Channel 5,6,8,9,10)
- Supports TWR, AoA, ToA, TDoA and PDoA
- Low external component count
- ARM® Cortex-M33 32bit processor
- ARM® TrustZone technology and S-DMA for security
- Supports AES, ECC, SHA, CRC and security interface
- Supports 1T1R/1T2R/1T3R transceiver architecture
- Complies with FCC & ETSI UWB spectral masks
- Maximum packet length of 1023 bytes for high data throughput applications
- Low power consumption design
- Data rates of 850 kbps, 6.81 Mbps, 7.8Mbps, 27.24Mbps and 31.2Mbps
- Integrated MAC support features
- Supports SPI(Master/Slave)/UART/I2C/JTAG/SWD/CAN interfaces
- Supports ROM, OTP and SRAM
- Dynamic programmable transmitter output power
- Integrated LDO, integrated RF frontend and matching network
- Supports automatic calibration
- Supports system clock or external crystal
- 5mm*5mm QFN 40 Pin package

Key Benefits

- Fully coherent receiver for maximum range and accuracy
- Asset location to an accuracy of 5cm
- High integration supports smallest customer BOM
- Integrated PMU, integrated RF frontend and matching network
- Low power consumption
- Radar performance to a resolution of 7.5cm
- AoA to an accuracy of 3°
- Supports automatic calibration
- Supports system clock or external crystal
- Small package: 5mm*5mm QFN

Applications

- Supports ranging, AoA, radar and data transmitting
- Supports TWR, ToA, TDoA and PDoA
- Supports radar:
  - ✓ Sentinel radar
  - ✓ Kicking radar
  - ✓ Child Presence Detection (CPD)
- Suitable for automotive market

1 IC DESCRIPTION

The CX500 is a fully integrated single impulse radio Ultra Wide Band (UWB) SoC chip compliant to IEEE802.15.4a HRP and IEEE802.15.4z HRP. It supports frame formats, which are compliant to IEEE 802.15.4a HRP UWB PHY and IEEE 802.15.4z HRP UWB PHY.

CX500 can be used in 2-way ranging or time difference of arrival (TDoA) location systems to determine distance to a precision of up to 5 cm and the angle of arrival (AoA) to a precision of up to 3°. It also supports data transfer rates up to 6.81 Mbit/s for base pulse repetition frequency (BPRF) and 31.2Mbit/s for higher pulse repetition frequency (HPRF).

CX500 consists of four major systems: core, baseband, RF and PMU. The core system is composed of Cortex-M33 processor, memory, and some common peripherals. The baseband system implements PHY-layer of UWB. The RF system completes the transmission and reception of RF signals. The PMU realizes power on/off process of the chip and low power management.

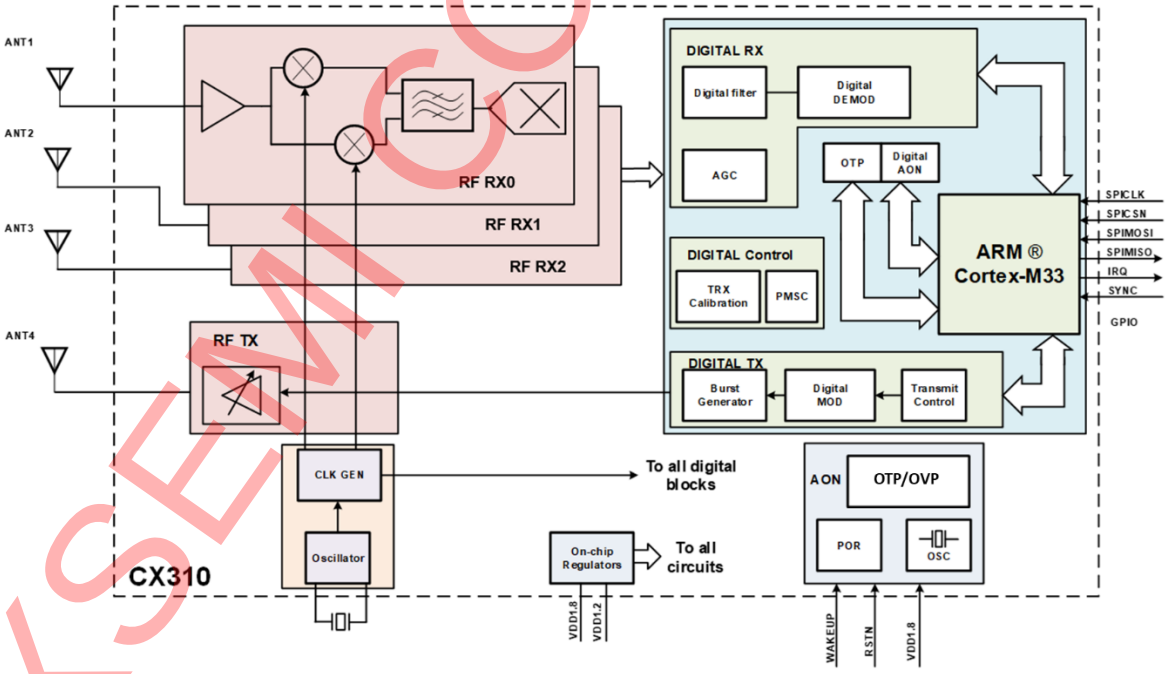

Figure 1: Block Diagram

The core sub-system consists of ARM Cortex M33, Busmatrix, DMA0, DMA1, CC312, CRC, SRAM, ROM, OTP, Cache, Peripherals (including QSPI, UART, I2C, Timer, RTC, GPIO, CAN, SSP, WDT, GPADC, etc.), and AON block.

A clock generator is used to provide the RF local oscillator signals for the RF frontend, digital baseband and SoC system.

Retention SRAM (32KB) can be used to retain CX500 configuration data during the lower power operational states when most of on-chip voltage regulators are disabled.

The host interface includes a SPI for device communications and configuration. A number of MAC features are implemented including CRC generation, CRC checking and receive frame filtering.

The CX500 baseband subsystem consists of TX, RX, Top Ctrl Module and Digital-Analog Interface. With these blocks, CX500 can handle the full baseband transmission/reception and encoding/decoding.

The baseband subsystem helps control the analog block, including power management, AGC, Calibration, and register config through APB. In addition to the basic transmission or reception, the baseband subsystem supports ranging, AoA (Angle of Arrival), radar and data transmitting function.

The RF RX amplifies the received signal in an ultra-wideband low-noise amplifier before down-converting it directly to analog baseband in three paths. A high-speed A/D converter is used to convert analog received signal to digital baseband. The baseband signal is demodulated and the resulting received data is made available to the Cortex-M33 processor.

An Automatic Gain Control is provided to ensure optimum receiver performance by adjusting receiver gain for changing signal and environmental conditions. The IC monitors the received signal level and makes appropriate automatic adjustments to ensure optimum receiver performance is maintained.

The transmit pulse train is generated by burst generator in digital transmitter. The pulse train is then pulse-shaped and amplified by RF TX which transmits channel-mask-compliant pulses to the external antenna. The transmit power is fully adjustable ensuring that the EIRP at the antenna is as close as possible to the maximum allowed.

The PMU subsystem realizes power on/off and low power management, supplied by VDD1/VDD2/VDD_IO, which can be divided into two main domains: aon domain and power down domain. Aon domain works all the time, and can retention system configuration, supplied by VDD1(1.8V). Power down domain can close the power in low power mode to save power, supplied by VDD2(1.2~1.8V). IO is supplied by VDD_IO (1.8V) independently.